REMARKS

Claims 1, 6, 7, 9-13, 15, 17, 18, 20-23, 25-27, 44, 52, 58, and 61-77 are pending. Claims 7, 17, 66, and 68 have been amended.

Claims 68-71 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 68 has been amended to address the Examiner's concerns, and particularly points out and distinctly claims the subject matter of the invention. Withdrawal of the 35 U.S.C. § 112, second paragraph, rejection of claim 68 and its dependent claims 69-71 is solicited.

Claim 44 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,275,184 to Nishizawa et al. This rejection is traversed.

Claim 44 recites a method for reducing the contaminants on a silicon wafer during a wet etching process. The method includes "immersing a wafer boat suspended on a lifting arm in an etching vessel having an aqueous hydrofluoric acid solution therein for a sufficient time to etch said silicon wafer" and "continuously feeding said aqueous hydrofluoric acid solution to process said semiconductor wafer." The method includes "stopping said continuous feeding of acid solution," and "rapidly removing said wafer boat from said etching vessel to remove surface contaminants residing on an upper surface of said aqueous hydrofluoric acid solution by an upward movement of said arm, thereby causing an upper portion of said aqueous hydrofluoric acid solution to spill out of said vessel to reduce the amount of said aqueous hydrofluoric acid solution in said etching vessel."

The reference to Nishizawa et al. discloses a wafer treatment method featuring continuous flow of treatment solutions. Nishizawa et al. does not disclose "stopping said continuous feeding of acid solution." Nishizawa et al. does not anticipate claim 44. Claim 44 is patentable over the cited reference to Nishizawa et al.

Claims 66 and 73 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,131,588 to Kamikawa et al. The rejection is traversed.

Claim 66 recites a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers. The method includes "immersing said semiconductor wafers in a semiconductor processing bath," and "rapidly removing an upper portion of a semiconductor processing fluid present in said etching bath by rapidly removing a wafer boat containing said wafers from said etching bath, to permit flow of said upper portion of said etching fluid out of said semiconductor etching bath and thereby break eddy currents holding said surface contaminants at said air/liquid interface."

The reference to Kamikawa et al. discloses a wafer processing apparatus in which a wafer boat is lifted out of an ozone water bath using a screw lift. The Kamikawa et al. reference contains no teaching of a method for removing contaminants by "rapidly removing an upper portion of a semiconductor processing fluid present in said etching bath by rapidly removing a wafer boat containing said wafers from said etching bath, to permit flow of said upper portion of said processing fluid out of said semiconductor bath and thereby break eddy currents holding said surface contaminants at said air/liquid interface." On the contrary, step 1413 of the process disclosed in the Kamikawa et al. reference, illustrated in Fig. 24, shows wafer W removed out of a deionized water (DIW) bath to the drying chamber 42 above bath 41. The DIW bath 41, with the wafer W removed, is shown to contain a maximum volume of DIW, and the overflow trough on the sides of the bath 41 contains no liquid. The Office Action states that the Kamikawa et al. reference discloses "rapidly removing an upper portion of a semiconductor processing fluid present in said etching bath by rapidly removing a wafer boat containing wafers from said bath," and points to Figs. 1-30 for support. Applicant respectfully submits that Figs. 1-30 contain no support for

this statement in the Office Action. Nothing in the Kamikawa et al. reference drawings or text teaches that any fluid has been removed out of the bath by lifting the wafer W, or that the wafer W is lifted rapidly. Notably, nothing in Kamikawa et al. teaches or suggests a process that removes contaminants contained in the DIW bath that has been used to rinse the wafer W. See col. 13, lines 19-42. The reference to Kamikawa et al. does not anticipate a wafer treatment method for removing contaminants that includes "rapidly removing an upper portion of a semiconductor processing fluid present in said etching bath by rapidly removing a wafer boat containing said wafers from said bath, to permit flow of said upper portion of said processing fluid out of said semiconductor bath." Claim 66 is patentable over the reference to Kamikawa et al.

Claim 73 recites a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers. The method includes "processing said semiconductor wafers in a semiconductor etching solution," and "rapidly removing an upper portion of said semiconductor etching solution by rapidly removing a wafer boat containing said wafers from said bath, to permit flow of said upper portion of said processing fluid and thereby break surface tension forces holding said surface contaminants at said air/liquid interface."

The reference to Kamikawa et al. discloses a wafer processing apparatus in which a wafer boat is lifted out of a water bath using a wafer guide mechanism 83 including a motor operating a threaded screw for lifting the wafer boat. The Kamikawa et al. reference contains no teaching of "rapidly removing an upper portion of said semiconductor etching solution by rapidly removing a wafer boat containing said wafers from said bath, to permit flow of said upper portion of said processing fluid and thereby break surface tension forces holding said surface contaminants at said air/liquid interface." On the contrary, in step 1413 of the process disclosed in the

Kamikawa et al. reference, illustrated in Fig. 24, wafer W is removed to the drying chamber 42 above DIW bath 41. Applicant notes that DIW is used to rinse processing fluid from the wafer W, and that DIW is not a semiconductor *etching* fluid. Further, no contaminants are shown or described in the reference to Kamikawa et al. as being contained in the DIW bath 41, and no solution is shown or described to have been removed from bath 41. The reference to Kamikawa et al. does not anticipate a wafer treatment method for removing contaminants that includes "rapidly removing an upper portion of said semiconductor etching solution by rapidly removing a wafer boat containing said wafers from said bath." Claim 73 is patentable over the reference to Kamikawa et al.

Claims 1, 6, 7, 9, 12, 15, 17, 18, 20, 22, 25, 26, 61, 64, 67, 68, 71, and 74-77 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishizawa et al. in view of U.S. Pat. No. 5,474,616 to Hayami et al. This rejection is traversed.

Claim 1 recites a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers. The method includes "immersing wafers in a bath of semiconductor processing fluid in a processing apparatus," "processing said wafers immersed in said bath of semiconductor processing fluid contained within said processing apparatus," and "reducing a liquid holding capacity of said processing apparatus, thereby rapidly displacing an upper portion of said bath of semiconductor processing fluid from said processing apparatus while said wafers remain fully immersed in a lower portion of said bath of semiconductor processing fluid within said processing apparatus to remove said surface contaminants from said air/liquid interface."

The reference to Nishizawa et al. discloses a method of wafer treatment by continuously and uniformly replacing solution in a constant-volume treatment bath. The Nishizawa et al. reference does not teach or suggest "reducing a liquid holding

capacity of said processing apparatus." Further, Nishizawa et al. does not teach or suggest "rapidly displacing an upper portion of said bath of semiconductor processing fluid from said processing apparatus while said wafers remain fully immersed in a lower portion of said bath of semiconductor processing fluid within said processing apparatus." The Examiner recognizes the deficiencies in Nishizawa et al. and cites Hayami et al. to provide what is missing.

The reference to Hayami et al. does not cure the deficiencies of the Nishizawa et al. reference. The Hayami et al. reference teaches a method for rinsing semiconductor wafers in which walls 20 are folded down to release treating fluid *prior to immersion* of the wafers being treated. The Hayami et al. reference does not teach or suggest "reducing a liquid holding capacity of said processing apparatus, thereby rapidly displacing an upper portion of said bath of semiconductor processing fluid from said processing apparatus while said wafers remain fully immersed in a lower portion of said bath of semiconductor processing fluid within said processing apparatus" as recited in claim 1. Claim 1 is not rendered obvious by the proposed combination of the references to Nishizawa et al. and Hayami et al.

Further, the proposed combination of the Nishizawa et al. and Hayami et al. references fails to establish *prima facie* obviousness for lack of motivation, which must come from the prior art, not applicant's disclosure. Nishizawa et al. discloses a fixed-volume wafer bath in which a uniformly rising flow of treatment solutions prevents contamination of the air/liquid interface. The wafer can be "put into and taken out of surface treatment without emptying wafer treatment bath 1." See col. 9, lines 4-6 of Nishizawa et al. Thus, the reference to Nishizawa et al. teaches away from a wafer treatment method that includes "reducing a liquid holding capacity of said processing apparatus, thereby rapidly displacing an upper portion of said bath of semiconductor processing fluid from said processing apparatus."

The reference to Hayami et al. discloses releasing side doors *prior to* immersion of the wafers into the bath, thus achieving the goal of removing floating particles "as soon as possible." See col. 2, lines 46-51. Further, Hayami et al. teaches that at the end of the rinsing process, "there are almost no particles P floating on the surface of the cleaning water 100. [...] Thus, when the semiconductor wafers 10 are lifted up, there are almost no particles adhering to the surfaces of each of the semiconductor wafers 10." See col. 6, lines 52-59. The wafers 10 are lifted up without any release of liquid by way of folding walls 20. Claim 1 and its dependent claim 6 are patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 7 recites a method for reducing contamination on a semiconductor wafer from a wet etching bath. The method includes "immersing said semiconductor wafer in said wet etching bath contained in a processing apparatus," and "processing said semiconductor wafer in said wet etching bath by continuously feeding an etching fluid." The method further includes "stopping the continuous feeding of said etching fluid," and "subsequently rapidly reducing a volume of said wet etching bath contained within said processing apparatus by removing an upper portion of said etching fluid from said processing apparatus to reduce an overall volume of fluid in said processing apparatus and remove surface contaminants from an air/liquid interface of said wet etching bath while retaining said semiconductor wafer fully immersed in a lower portion of said etching fluid contained within said processing apparatus." The method also includes "subsequently removing said semiconductor wafer from said wet etching bath."

The reference to Nishizawa et al. discloses a method of wafer treatment by continuously and uniformly replacing solution in a constant-volume treatment bath. The Nishizawa et al. reference does not teach or suggest "stopping the continuous feeding of said etching fluid," and "subsequently rapidly reducing a volume of said

wet etching bath contained within said processing apparatus by removing an upper portion of said etching fluid from said processing apparatus to reduce an overall volume of fluid in said processing apparatus."

The reference to Hayami et al. does not cure the deficiencies of Nishizawa et al. As noted above, the method of removing contaminants disclosed by the Hayami et al. reference involves opening a door in the processing vessel prior to immersion of the wafers. The Hayami et al reference does not teach or suggest "subsequently rapidly reducing a volume of said wet etching bath contained within said processing apparatus by removing an upper portion of said etching fluid from said processing apparatus to reduce an overall volume of fluid in said processing apparatus and remove surface contaminants from an air/liquid interface of said wet etching bath while retaining said semiconductor wafer fully immersed in a lower portion of said etching fluid contained within said processing apparatus." The Office Action seems to recognize this deficiency when it states that the Hayami et al. reference discloses removing etching fluid "by hingedly releasing a door located at an upper portion of the bath that *allows* reducing a liquid holding capacity...while the wafer remain (sic) fully immersed..." See the last paragraph on page 5 of the Office Action. Applicant notes, however, that the reference to Hayami et al. does not disclose that the door is released while the wafer remains fully immersed. Further, it is insufficient for a rejection base on obviousness that the prior art *could be* modified to derive the claimed invention. Although the prior art device "may be capable of being modified to run the way [the applicant's] apparatus is claimed, there must be a suggestion or motivation in the reference to do so." In re Mills, 916 F.2d 680 (Fed. Cir. 1990). The cited prior art contains no suggestion or motivation to modify the method disclosed in the Hayami et al. reference to derive the present invention.

Further, there is no motivation in the prior art to modify Nishizawa et al. to provide a method that includes "stopping the continuous feeding of said etching fluid" and "subsequently rapidly reducing a volume of said wet etching bath contained within said processing apparatus by removing an upper portion of said etching fluid from said processing apparatus to reduce an overall volume of fluid in said processing apparatus.". On the contrary, Nishizawa et al. specifically relates to a constant volume, uniform flow process, and thus teaches away from a process that includes "rapidly reducing a volume of said wet etching bath." Claim 7 and its dependent claims 9, 10, and 13 are patentable over the references to Nishizawa et al. and Hayami et al.

Claim 12 recites a method for removing surface contaminants from an air/liquid interface of a semiconductor processing cleaning bath for processing semiconductor wafers. The method includes "immersing said semiconductor wafers in said semiconductor processing cleaning bath contained in a processing apparatus," and "reducing a volume of fluid in said semiconductor processing cleaning bath before removing said semiconductor wafers by rapidly removing from a top of said processing apparatus an upper portion of a semiconductor processing fluid present in said bath while said wafers are in said bath, by hingedly releasing a door located at an upper portion of said processing apparatus to rapidly reduce a liquid holding capacity of said processing apparatus and to remove said surface contaminants from said air/liquid interface."

The reference to Nishizawa et al. discloses a method of wafer treatment by continuously and uniformly replacing solution in a constant-volume treatment bath. The Nishizawa et al. reference does not teach or suggest "reducing a volume of fluid in said semiconductor processing cleaning bath before removing said semiconductor wafers by rapidly removing from a top of said processing apparatus an upper portion of a semiconductor processing fluid present in said bath while said wafers are in said

bath." Further, Nishizawa et al. does not teach or suggest removing "an upper portion of the semiconductor processing fluid," "by hingedly releasing a door located at an upper portion of said processing apparatus to rapidly reduce a liquid holding capacity of said processing apparatus and to remove said surface contaminants from said air/liquid interface." The Examiner recognizes the deficiencies in Nishizawa et al. and cites Hayami et al. to provide what is missing.

The reference to Hayami et al. does not cure the deficiencies of Nishizawa et al. The reference to Hayami et al. teaches a method for rinsing wafers in which folding walls 20 are folded down to release treating fluid *prior to immersion* of the wafers being treated. The Hayami et al. reference does not teach or suggest removing a volume of treatment water "while said wafers are in said bath" as recited in the claim 12. The reference to Hayami et al. does not teach or suggest a process that includes "immersing said semiconductor wafers in said semiconductor processing cleaning bath," and "reducing a volume of fluid in said semiconductor processing cleaning bath before removing said semiconductor wafers."

Moreover, as noted above in connection with claim 7, the proposed combination of Nishizawa et al. and Hayami et al. fails to establish *prima facie* obviousness of claim 12. The proposed combination lacks motivation, which must come from the prior art, not applicant's disclosure. Nishizawa et al. discloses a fixed-volume wafer bath in which a uniformly rising flow of treatment solutions prevents contamination of the air/liquid interface, and so teaches away from a method "to rapidly reduce a liquid holding capacity of [a] processing apparatus." The reference to Hayami et al. discloses releasing side doors *prior to* immersion of the wafers into the bath. It is not sufficient for a rejection based on obviousness that a reference *could be* modified to derive the claimed invention. The cited prior art does not provide the requisite suggestion or motivation to modify the process to include releasing the doors

after immersion of the wafers. The suggestion to do so comes only from Applicant's disclosure as part of an improper hindsight attempt to reconstruct the invention. Claim 12 is patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 15 recites a method for removing surface contaminants from an air/liquid interface of a semiconductor processing cleaning bath for processing semiconductor wafers. The method includes "immersing said wafers in said semiconductor processing cleaning bath," and "reducing a volume of fluid in said semiconductor processing cleaning bath by rapidly removing an upper portion of a semiconductor processing fluid present in said bath from said processing apparatus, while said wafers are immersed in said bath." This is done "by telescopically collapsing sidewalls of a vessel containing said bath to rapidly reduce a liquid holding capacity of said processing apparatus and to remove said surface contaminants from said air/liquid interface." The Examiner recognizes deficiencies in the Nishizawa et al. reference, and relies on the reference to Hayami et al. to provide what is missing.

The Hayami et al. reference does not cure the deficiencies of the reference to Nishizawa et al. The Office Action asserts that "telescopically collapsing sidewalls" are shown in Figs. 41 and 42 of the reference to Hayami et al. Applicant respectfully disagrees, as noted in the prior response dated March 25, 2004. Further, for reasons analogous to those set forth above in connection with claims 7 and 12, the proposed combination of the references to Hayami et al. and Nishizawa et al. does not establish *prima facie* obviousness of a method that includes "reducing a volume of fluid in said semiconductor processing cleaning bath by rapidly removing an upper portion of a semiconductor processing fluid present in said bath from said processing apparatus, while said wafers are immersed in said bath, by telescopically collapsing sidewalls of a vessel containing said bath to rapidly reduce a liquid holding capacity of said processing apparatus and to remove said surface contaminants from said air/liquid

interface." Claim 15 is patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 17 recites a method for etching a semiconductor wafer. The method includes "placing an aqueous hydrofluoric acid etching fluid into a wet etching vessel," and "immersing said semiconductor wafer in a process volume of said etching fluid." The method also includes "contacting said semiconductor wafer with said etching fluid for a predetermined time," and "reducing an overall volume of fluid contained in said wet etching vessel by rapidly removing an upper portion of said etching fluid from the top of said wet etching vessel while keeping said semiconductor wafer immersed to obtain a remaining portion of said etching fluid." The remaining portion has "a smaller volume than said process volume." The semiconductor wafer is then removed "from said remaining portion of said etching fluid."

As noted above, the reference to Nishizawa et al. discloses a fixed volume, continuous flow method of wafer treatment. The reference to Nishizawa et al. does not teach or suggest "reducing an overall volume of fluid contained in said wet etching vessel by rapidly removing an upper portion of said etching fluid from the top of said wet etching vessel while keeping said semiconductor wafer immersed to obtain a remaining portion of said etching fluid," such that the remaining portion has "a smaller volume than said process volume."

The reference to Hayami et al. does not cure the deficiencies of the Nishizawa et al. reference. The Hayami et al. reference discloses a method of wafer treatment in which a door is released to evacuate processing fluid prior to immersion of wafers. The Hayami et al. reference does not teach or suggest "reducing an overall volume of fluid contained in said wet etching vessel by rapidly removing an upper portion of said etching fluid from the top of said wet etching vessel *while keeping said semiconductor wafer immersed.*" Further, the proposed combination of the Nishizawa et al. and

Hayami et al. references does not establish *prima facie* obviousness for reasons analogous to those set forth above in connection with claims 1, 7, 12, and 15. Claim 17 and its dependent claims 18, 20, 26, and 27 are patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 21 recites a method for etching a semiconductor wafer. The method includes "placing an etching fluid into a wet etching vessel," "placing said semiconductor wafer in said etching fluid," and "contacting said semiconductor wafer with said etching fluid for a predetermined time." The method also includes "reducing a liquid holding capacity of said wet etching vessel, thereby rapidly removing a portion of said etching fluid from the top of said wet etching vessel by opening a valve to reduce rapidly an overall volume of fluid in said wet etching vessel while said semiconductor wafer remains immersed in a lower portion of said etching fluid."

The reference to Nishizawa et al. discloses a fixed volume, continuous flow wafer treatment method. The Nishizawa et al. reference does not teach or suggest a wafer treatment method that includes "reducing a liquid holding capacity of said wet etching vessel, thereby rapidly removing a portion of said etching fluid from the top of said wet etching vessel by opening a valve to reduce rapidly an overall volume of fluid in said wet etching vessel."

The reference to Hayami et al. does not cure the deficiencies of Nishizawa et al. The Hayami et al. reference discloses a method of wafer treatment in which a door is released prior to immersion of wafers. The Hayami et al. reference does not teach or suggest "reducing a liquid holding capacity of said wet etching vessel, thereby rapidly removing a portion of said etching fluid from the top of said wet etching vessel by opening a valve to reduce rapidly an overall volume of fluid in said wet etching vessel while said semiconductor wafer remains immersed in a lower portion of said etching

fluid." Claim 21 is patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 22 recites a method for etching a semiconductor wafer. The method includes "placing an etching fluid into a wet etching vessel," "immersing said semiconductor wafer in said etching fluid," "contacting said semiconductor wafer with said etching fluid for a predetermined time," and "rapidly removing a portion of said etching fluid from an upper surface of said wet etching vessel by hingedly releasing a door located at an upper portion of said wet etching vessel to reduce a liquid holding capacity of said wet etching vessel while said semiconductor wafer remains immersed in a lower portion of said etching fluid."

The reference to Nishizawa et al. discloses a method of treating wafers using a uniform, upward flow of treatment solutions in a vessel having a fixed volume. The Examiner admits that Nishizawa et al. does not disclose "rapidly removing a portion of said etching fluid from the upper surface of said wet etching vessel by hingedly releasing a door located at an upper portion of said wet etching vessel" and relies on Hayami et al. to supply what is missing.

The Hayami et al. reference does not cure the deficiencies of the reference to Nishizawa et al. The Hayami et al. reference discloses a method of wafer treatment in which folding walls 20 are folded down to release treating fluid *prior to immersion* of the wafers being treated. The reference to Hayami et al. does not teach or suggest "rapidly removing a portion of said etching fluid from the upper surface of said wet etching vessel by hingedly releasing a door located at an upper portion of said wet etching vessel to reduce a liquid holding capacity of said wet etching vessel *while said semiconductor wafer remains immersed* in a lower portion of said etching fluid," as recited in claim 22.

Further, the proposed combination of the references to Nishizawa et al. and Hayami et al. lacks the requisite motivation, which must come from the prior art, not applicant's disclosure. The fixed volume vessel of the reference to Nishizawa et al. is used in a process in which a uniformly rising flow of treatment solution prevents contamination of the air/liquid interface. The wafer can be "put into and taken out of surface treatment without emptying wafer treatment bath 1." See col. 9, lines 4-6 of the Nishizawa et al. reference. Thus, the reference to Nishizawa et al. provides no motivation for modifying the wafer treatment device or method to include the folding doors of the reference to Hayami et al.

The Hayami et al. reference also lacks a suggestion or motivation to combine and modify the references as required to derive the present invention. The reference to Hayami et al. discloses releasing the side doors *prior to immersion* of the wafers in the bath, thus achieving the goal of removing floating particles "as soon as possible." See col. 2, lines 46-51. Further, the Hayami et al. reference teaches that at the end of the rinsing process "there are almost no particles P floating on the surface of the cleaning water 100. [...] Thus, when the semiconductor wafers 10 are lifted up, there are almost no particles adhering to the surfaces of each of the semiconductor wafers 10." See col. 6, lines 52-59. The cited references to Nishizawa et al. and Hayami et al. do not suggest the desirability of "rapidly removing from a top of said processing apparatus an upper portion of a semiconductor processing fluid present in said bath while said wafers are in said bath." The proposed combination of the Nishizawa et al. and Hayami et al. references lacks the motivation required to combine the references and derive the process as recited in claim 22.

The Office Action states that one of skill in the art would be motivated to modify Nishizawa et al. based on Hayami et al. "because use of the door would have provided removing of contaminants from the top of the wafer etching bath when the

door opened." This broad, conclusory statement is not evidence, however, and begs the question. The method disclosed by the Hayami et al. reference must be modified to derive the present invention, and there must be motivation to do so in the prior art. It is not sufficient that the prior art apparatus *could be* modified to derive an apparatus that performs the recited method steps. There must be some motivation in the prior art, not just from applicant's disclosure, to suggest that steps disclosed in the prior art can be modified as required to derive applicant's invention. Such motivation is lacking in the prior art of record.

Further, even if Nishizawa et al. were properly combinable with Hayami et al., the result would involve a method in which doors are used to release bath liquid prior to immersion of wafers, which is not the present invention as recited in claim 22. Claim 22 is patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 25 recites a method for etching a semiconductor wafer. The method includes "placing an aqueous hydrofluoric acid solution into a wet etching vessel," "immersing said semiconductor wafer in said aqueous hydrofluoric acid solution," "contacting said semiconductor wafer with said aqueous hydrofluoric acid solution for a predetermined time," and "reducing a fluid-containing volume of said wet etching vessel so as to rapidly displace a portion of said aqueous hydrofluoric acid solution from an upper portion of said wet etching vessel by telescopically collapsing sidewalls of said wet etching vessel, said semiconductor wafer remaining immersed in a remaining portion of said aqueous hydrofluoric acid solution."

The reference to Nishizawa et al. contains no teaching or suggestion of treating wafers in a wet etching vessel by "reducing a fluid-containing volume of said wet etching vessel." Nishizawa et al. also contains no teaching or suggestion of treating the wafers "so as to rapidly displace a portion of said aqueous hydrofluoric acid solution from an upper portion of said wet etching vessel by telescopically collapsing

sidewalls of said wet etching vessel, said semiconductor wafer remaining immersed in a remaining portion of said aqueous hydrofluoric acid solution."

Recognizing the deficiencies of Nishizawa et al., the Examiner relies on Hayami et al., but Hayami et al. discloses folding doors, not telescoping doors, which release treatment fluid *prior to* immersing wafers in a treatment bath, not while the wafers remain immersed. Further, the proposed combination lacks the requisite motivation to establish *prima facie* obviousness. As noted above in connection with claim 22, Nishizawa et al. uses a fixed-volume vessel in a method that prevents surface contamination, and Hayami et al. releases treatment solution using folding doors prior to immersion of the wafers. The proposed modification of the references finds no motivation, other than that provided by applicant. Moreover, the proposed combination, even if proper, does not produce the invention of claim 25. Claim 25 is patentable over the references to Nishizawa et al. and Hayami et al.

Claim 61 recites a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers. The method includes "immersing said semiconductor wafers in said semiconductor processing bath contained in a processing apparatus," and "reducing a volume of said semiconductor processing bath contained within said processing apparatus by rapidly removing an upper portion of said semiconductor processing bath present in said processing apparatus, while said semiconductor wafers are immersed in a remaining lower portion of said semiconductor processing bath, to permit flow of said upper portion of said processing bath out of said processing apparatus and reduce a total volume of liquid contained within said processing apparatus and thereby break eddy currents holding said surface contaminants at said air/liquid interface."

The reference to Nishizawa et al. discloses a wafer treatment process performed in wafer bath 1, which has a fixed volume. Treatment solutions flow through supply line 3 into the base of wafer bath 1. Treatment is conducted continuously by changing the solution flowing upwardly into the wafer bath 1. Wafers are lifted out of the wafer bath 1 at treatment completion "without emptying wafer treatment bath 1." See col. 9, lines 4-6. The Nishizawa et al. reference does not teach a wafer treatment method that includes "reducing a volume of said semiconductor processing bath contained within said processing apparatus by rapidly *removing* an upper portion of said semiconductor processing bath present in said processing apparatus, while said semiconductor wafers are immersed in a remaining lower portion of said semiconductor processing bath, to permit flow of said upper portion of said processing bath out of said processing apparatus and *reduce a total volume* of liquid *contained within* said processing apparatus." Furthermore, Nishizawa et al. does not teach such a method that will "thereby break eddy currents holding said surface contaminants at said air/liquid interface." The Examiner refers generally to Fig. 2 for support of the rejection, but Fig. 2 shows a processing bath contained within wafer bath 1 having a constant volume of fluid. The reference to Nishizawa et al. does not disclose a wafer process including steps to "reduce a total volume of liquid *contained within*" wafer bath 1, and so does not anticipate claim 61 and its dependent claims 62-64 and 67.

Hayami et al. does not cure the deficiencies of Nishizawa et al. Hayami et al. has been cited as providing a hingedly releasing door, as recited in claim 64, or telescopically collapsing sidewalls, as recited in claim 67. The process of Hayami et al., however, is distinct from that of the present invention, in that treatment liquid is released according to the process described in Hayami et al. *prior to immersion* of the wafers. Hayami et al. does not teach or suggest a wafer treatment method that includes "immersing said semiconductor wafers in said semiconductor processing bath contained in a processing apparatus," and "reducing a volume of said semiconductor

processing bath contained within said processing apparatus by rapidly removing an upper portion of said semiconductor processing bath present in said processing apparatus, *while said semiconductor wafers are immersed* in a remaining lower portion of said semiconductor processing bath." Further, with respect to claim 67, Hayami et al. does not teach telescoping sidewalls, as discussed above in connection with claims 15 and 25. Claim 61 and dependent claims 62-64 and 67 are patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 68 recites "a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers." The method includes "processing said semiconductor wafers in a semiconductor processing bath having a processing bath volume contained in a vessel," and "reducing said processing bath volume of said semiconductor processing bath in a processing vessel by rapidly removing an upper portion of said semiconductor processing bath present in said vessel, while said wafers are immersed in a remaining lower portion of said semiconductor processing bath, to permit flow of said upper portion of said processing bath out of said vessel and thereby break surface tension forces holding said surface contaminants at said air/liquid interface, an overall volume of liquid remaining in said vessel being less than said processing bath volume." The method also includes "removing said semiconductor wafers from said lower portion of said semiconductor processing bath remaining in said vessel."

The fixed volume, continuous flow treatment method disclosed in the reference to Nishizawa et al. does not teach or suggest reducing a "processing bath volume of said semiconductor processing bath in a processing vessel by rapidly removing an upper portion of said semiconductor processing bath present in said vessel" with "an overall volume of liquid remaining in said vessel being less than said processing bath volume."

The reference to Hayami et al. does not cure the deficiencies of the Nishizawa et al. reference. Opening a door to release treatment fluid *prior to* wafer immersion, as disclosed in the Hayami et al. reference, does not anticipate or render obvious a method of "reducing said processing bath volume of said semiconductor processing bath in a processing vessel by rapidly removing an upper portion of said semiconductor processing bath present in said vessel, while said *wafers are immersed* in a remaining lower portion of said semiconductor processing bath." Claim 68 and dependent claims 69-71 and 74 are patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 75 recites a method for reducing the contamination on a semiconductor wafer from a wet etching bath. The method includes "processing said semiconductor wafer in said wet etching bath containing an etching fluid," "subsequently reducing a volume of etching fluid in said wet etching bath and breaking eddy currents of said wet etching bath by rapidly removing an upper portion of said etching fluid from a processing vessel containing said wet etching bath to reduce an overall volume of fluid contained within said processing vessel, said act of breaking said eddy currents further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents," and "subsequently removing said semiconductor wafer from said reduced overall volume of fluid."

The reference to Nishizawa et al. discloses a <u>fixed</u> volume, continuous flow wafer treatment process. The Nishizawa et al. reference does not teach or suggest a method that includes "reducing a volume of etching fluid in said wet etching bath and breaking eddy currents of said wet etching bath by rapidly removing an upper portion of said etching fluid from a processing vessel containing said wet etching bath to *reduce an overall volume of fluid* contained within said processing vessel."

The reference to Hayami et al. does not cure the deficiencies of the reference to Nishizawa et al. The Hayami et al. reference discloses a process in which fluid is released from a treatment vessel prior to immersion of the wafers. The reference to Hayami et al. does not teach "processing said semiconductor wafer in said wet etching bath containing an etching fluid," "subsequently reducing a volume of etching fluid in said wet etching bath and breaking eddy currents of said wet etching bath by rapidly removing an upper portion of said etching fluid from a processing vessel containing said wet etching bath to reduce an overall volume of fluid contained within said processing vessel," and "subsequently removing said semiconductor wafer from said reduced overall volume of fluid." It is not enough that the disclosure of the Hayami et al. reference *could be* modified to derive the present invention. The reference to Hayami et al., however, also does not contain the requisite suggestion or motivation for modifying the disclosure as would be necessary to derive the present invention and establish a *prima facie* obviousness rejection. Claim 75 is patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 76 recites a method for reducing the contamination on a semiconductor wafer from a wet etching bath. The method includes "processing said semiconductor wafer in said wet etching bath containing an etching fluid completely filling a processing vessel," and "subsequently reducing a volume of said etching fluid and breaking surface tension forces of said wet etching bath by rapidly removing an upper portion of said etching fluid from said processing vessel containing said wet etching bath and reduce an overall volume of fluid contained within said processing vessel such that said processing vessel is no longer full." The "act of breaking said surface tension forces further" releases "surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents." The method includes "subsequently removing said semiconductor wafer from said wet etching bath having a reduced overall volume of fluid."

The reference to Nishizawa et al. discloses a fixed volume continuous flow wafer treatment process. The treatment vessel is constantly full of treatment liquid in which the wafers are immersed. The Nishizawa et al. reference does not teach or suggest etching wafers using etching fluid in an etching bath contained in a processing vessel and "subsequently reducing a volume of said etching fluid and breaking surface tension forces of said wet etching bath by rapidly removing an upper portion of said etching fluid from said processing vessel containing said wet etching bath and reduce an overall volume of fluid contained within said processing vessel such that said processing vessel is *no longer full*."

The reference to Hayami et al. does not cure the deficiencies of the Nishizawa et al. reference. The Hayami et al. reference discloses releasing treatment fluid from a processing vessel *prior* to wafer immersion. The reference to Hayami et al. does not teach or suggest "processing said semiconductor wafer in said wet etching bath containing an etching fluid completely filling a processing vessel," "subsequently reducing a volume of said etching fluid and breaking surface tension forces of said wet etching bath by rapidly removing an upper portion of said etching fluid from said processing vessel containing said wet etching bath and reduce an overall volume of fluid contained within said processing vessel such that said processing vessel is no longer full," and "subsequently removing said semiconductor wafer from said wet etching bath having a reduced overall volume of fluid." Claim 76 is patentable over the cited references to Nishizawa et al. and Hayami et al.

Claim 77 recites a method for reducing the contamination on a semiconductor wafer. The method includes "processing said semiconductor wafer immersed in a static etching bath containing an etching fluid," and "reducing a volume of said etching fluid by rapidly removing an upper portion of said etching fluid from a container holding said static etching bath to reduce an overall volume of fluid

contained within said container, such that said container holds less fluid while said semiconductor wafer is immersed in a remaining portion of said static etching bath."

The reference to Nishizawa et al. discloses a continuous flow wafer treatment process. The Nishizawa et al. reference does not teach or suggest "processing said semiconductor wafer immersed in a static etching bath." The Nishizawa et al. reference also discloses a fixed volume treatment process. The Nishizawa et al. reference does not teach or suggest "reducing a volume of said etching fluid by rapidly removing an upper portion of said etching fluid from a container holding said static etching bath to reduce an overall volume of fluid contained within said container, such that said container holds less fluid."

The reference to Hayami et al. does not cure the deficiencies of the Nishizawa et al. reference. The Hayami et al. reference discloses reducing a volume of wafer treatment fluid prior to wafer immersion. The reference to Hayami et al. does not teach or suggest "reducing a volume of said etching fluid by rapidly removing an upper portion of said etching fluid from a container holding said static etching bath to reduce an overall volume of fluid contained within said container, such that said container holds less fluid *while said semiconductor wafer is immersed* in a remaining portion of said static etching bath." Claim 77 is patentable over the cited references to Nishizawa et al. and Hayami et al.

Applicant notes that the grounds of rejection in the Office Action are not new as to claims 12, 15, 22, 25, 64, and 67, however, the Office Action does not respond to the respective traverses contained in applicant's response dated March 25, 2004. Remarks from applicant's response related to the cited prior art, not repeated here for the sake of brevity, are incorporated as applicable to the present rejections.

Applicant urges entry of this after-final amendment. The claim amendments are intended to present the claims in better form for allowance. The amendments are necessary to eliminate ambiguities in the claims, and to address the Examiner's concerns related to indefiniteness which were newly raised in the prior Office action.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: June 18, 2004

Respectfully submitted,

By _____

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